



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Re the Application of: HASHIMOTO, Hiroshi et al.

Serial No.: 09/960,399

Filed: September 24, 2001

Group Art Unit: 2814

Examiner: Howard Weiss

P.T.O. Confirmation No.: 5652

For. A SEMICONDUCTOR INTEGRATED CIRCUIT AND FABRICATION PROCESS  
HAVING COMPENSATED STRUCTURES TO REDUCE MANUFACTURING DEFECTS  
(as amended)

INFORMATION DISCLOSURE STATEMENT  
PURSUANT TO 37 CFR 1.97(c)

Commissioner for Patents  
Washington, D.C. 20231

October 1, 2002

Sir:

The attention of the Patent and Trademark Office is hereby directed to the documents listed on the attached Form PTO-1449. One copy of each of these documents is attached.

This Information Disclosure Statement is being submitted after issuance of a first official action on the merits and expiration of the three month period following the filing date or the entry of the national stage for the above-captioned application, but prior to issuance of either a final official action or a Notice of Allowance. A check is attached hereto which covers the \$ 180.00 fee set forth in 37 CFR 1.17(p).

The above information is presented so that the Patent and Trademark Office can, in the first instance, determine any materiality thereof to the claimed invention. See 37 CFR 1.104(a) concerning the PTO duty to consider and use any such information. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the

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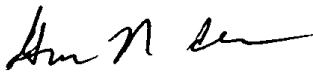
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documents cited in the attached Form PTO-1449 be made of record therein and appear on the first page of any patent to issue therefrom.

The Commissioner is hereby authorized to charge any additional fee (or credit any overpayment) associated with this statement to our Deposit Account No. 01-2340. Two copies of this authorization are attached.

Respectfully submitted,

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Enclosures: PTO-1449 and references (2)  
Check for \$ 180.00